

| Course Number | COE328 |
| --- | --- |
| Course Title | Digital Systems - F2022 |
| Semester/Year | Fall 2022 |
| Instructor | Shazzat Hossain |
| TA Name | Sajjad |

| Lab/Tutorial Report No. | Lab 3 |
| --- | --- |

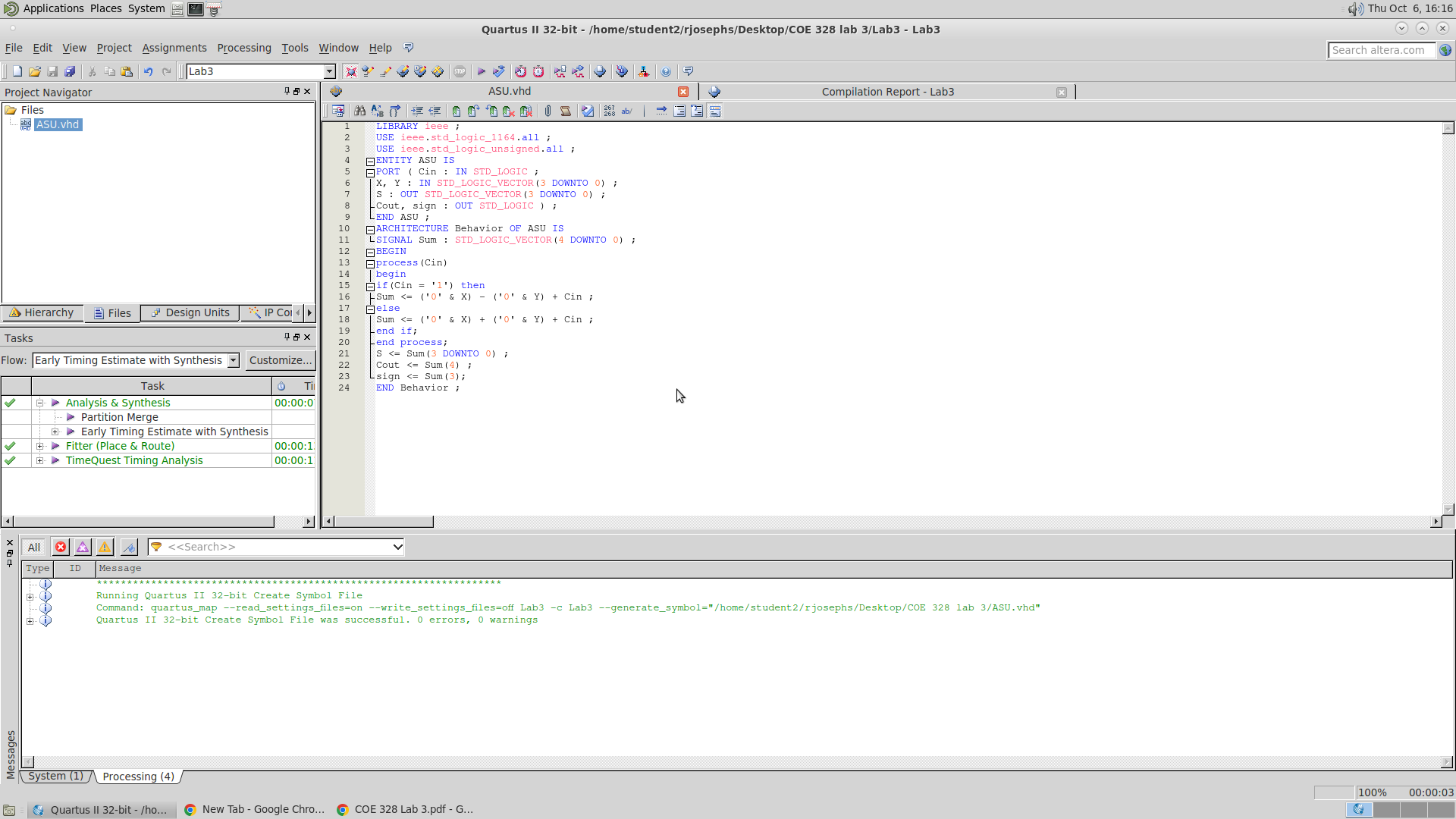
| Report Title | **Lab 3 - Adder and Subtractor Unit** |
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| Section No. | 11 |
| --- | --- |
| Group No. | N/A |
| Submission Date | Oct 17, 2022 |
| Due Date | Oct 21, 2022 |

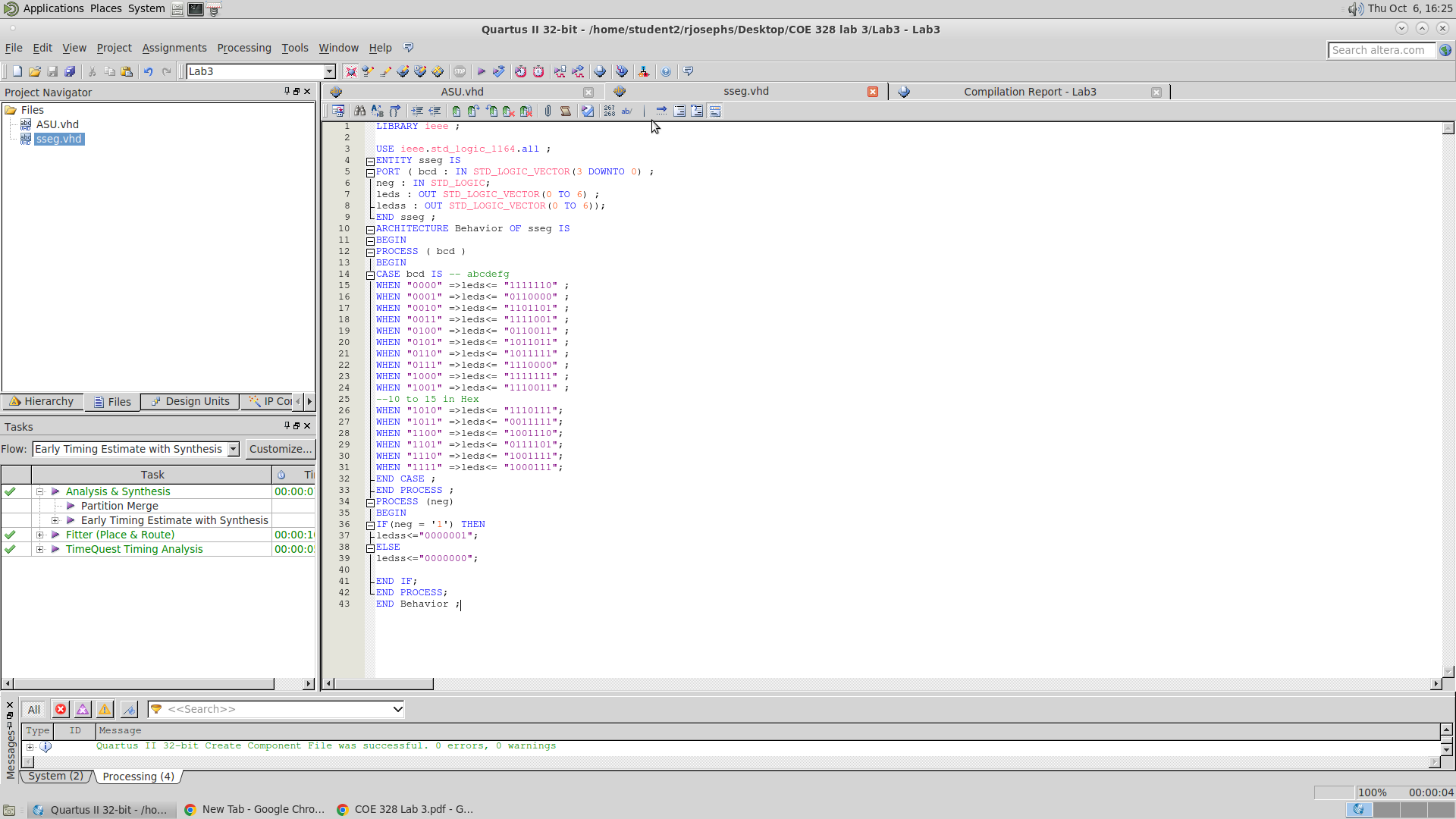
| Student Name | Student ID | Signature\* |
| --- | --- | --- |
| [Hamza Malik](mailto:hamza.ejaz.malik@torontomu.ca) | 501112545 | Hamza Malik |

*\*By signing above you attest that you have contributed to this submission and confirm that all work you have contributed to this submission is your own work. Any suspicion of copying or plagiarism in this work will result in an investigation of Academic Misconduct and may result in a “0” on the work, an “F” in the course, or possibly more severe penalties, as well as a Disciplinary Notice on your academic record under the Student Code of*

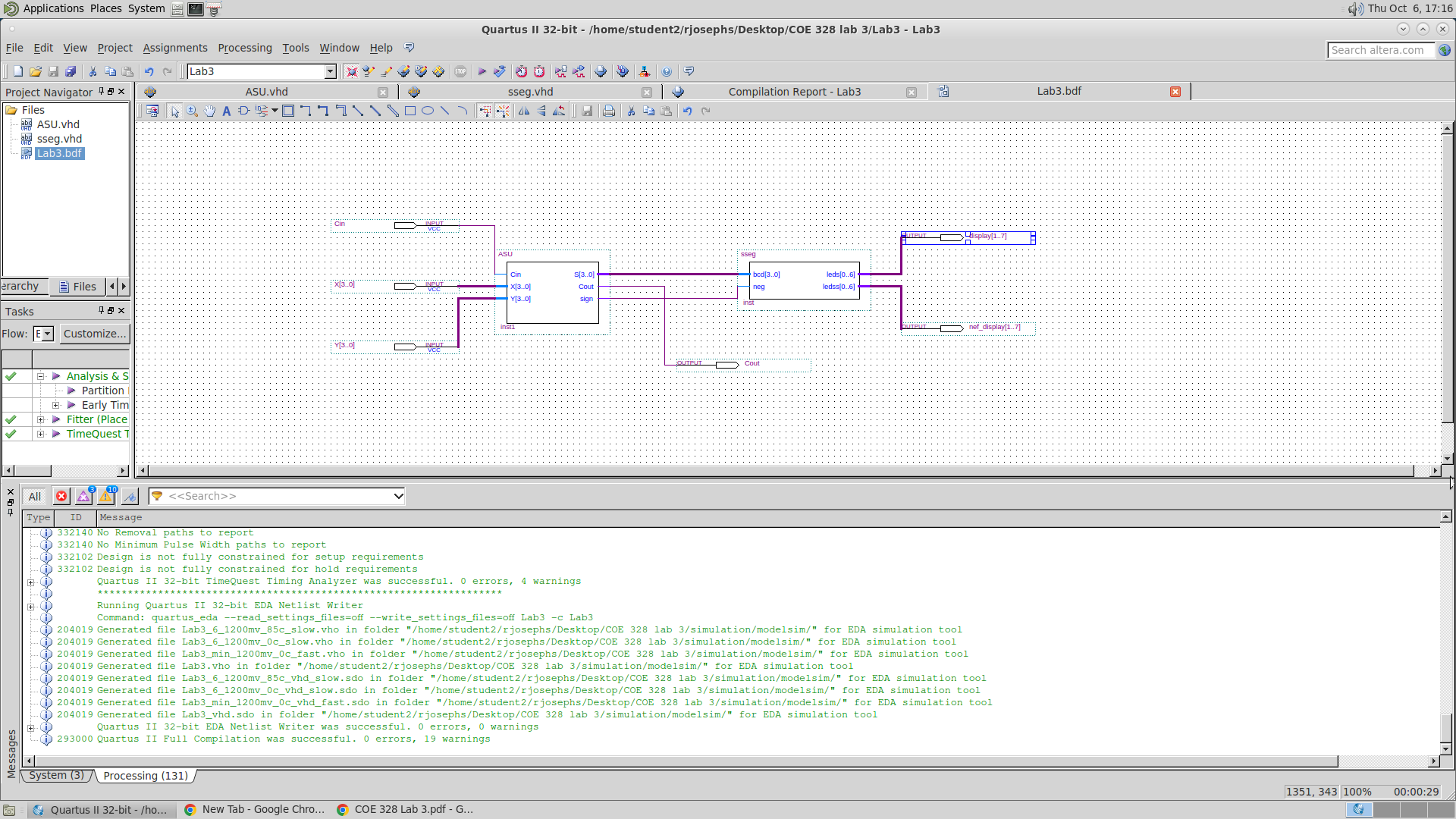
This is our vdhl Skeleton code from figure 5.28 for part 1 of lap 3

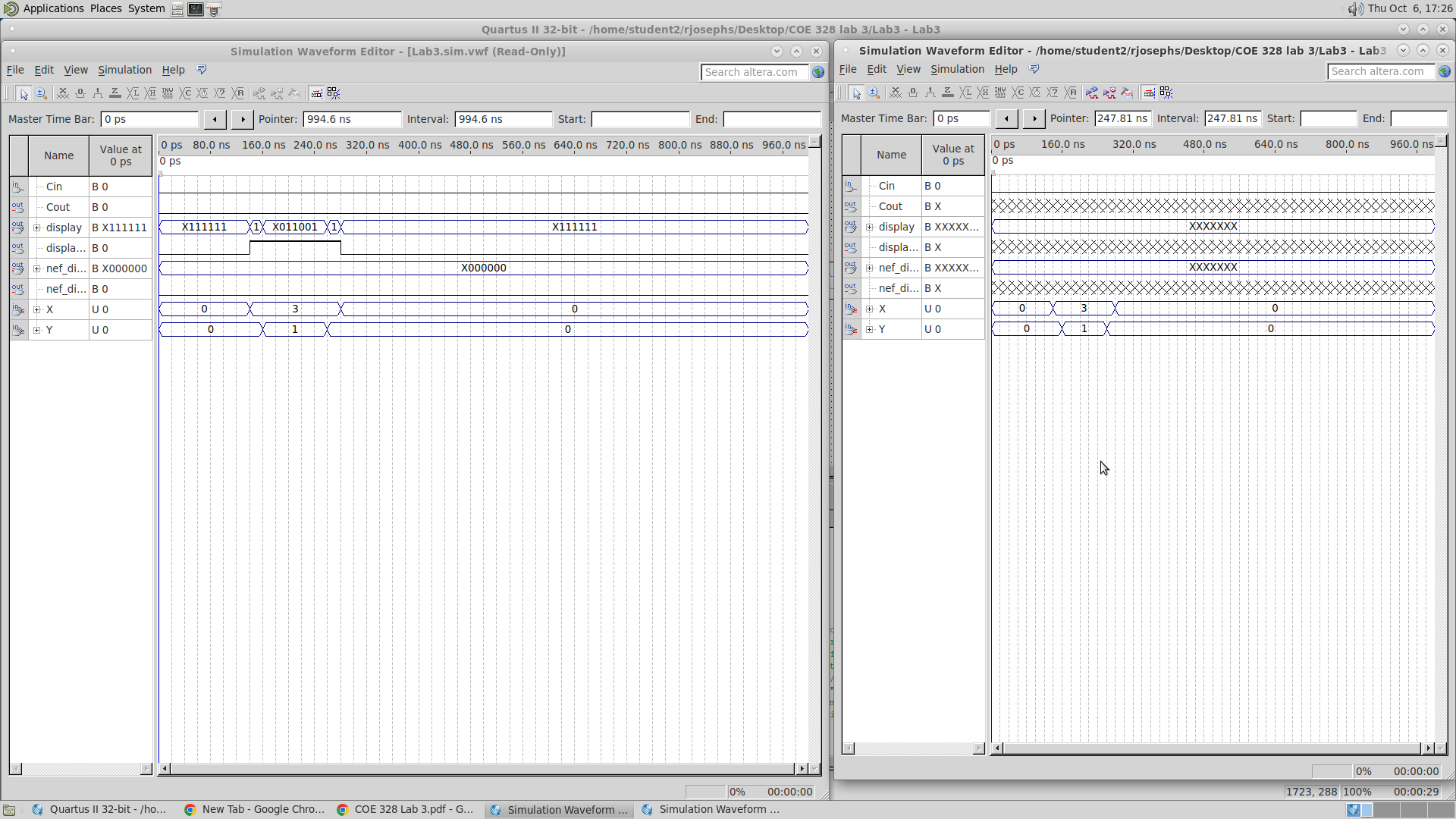
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This is our vhd Skeleton code from figure 6.47 for part 1 of lap 3.

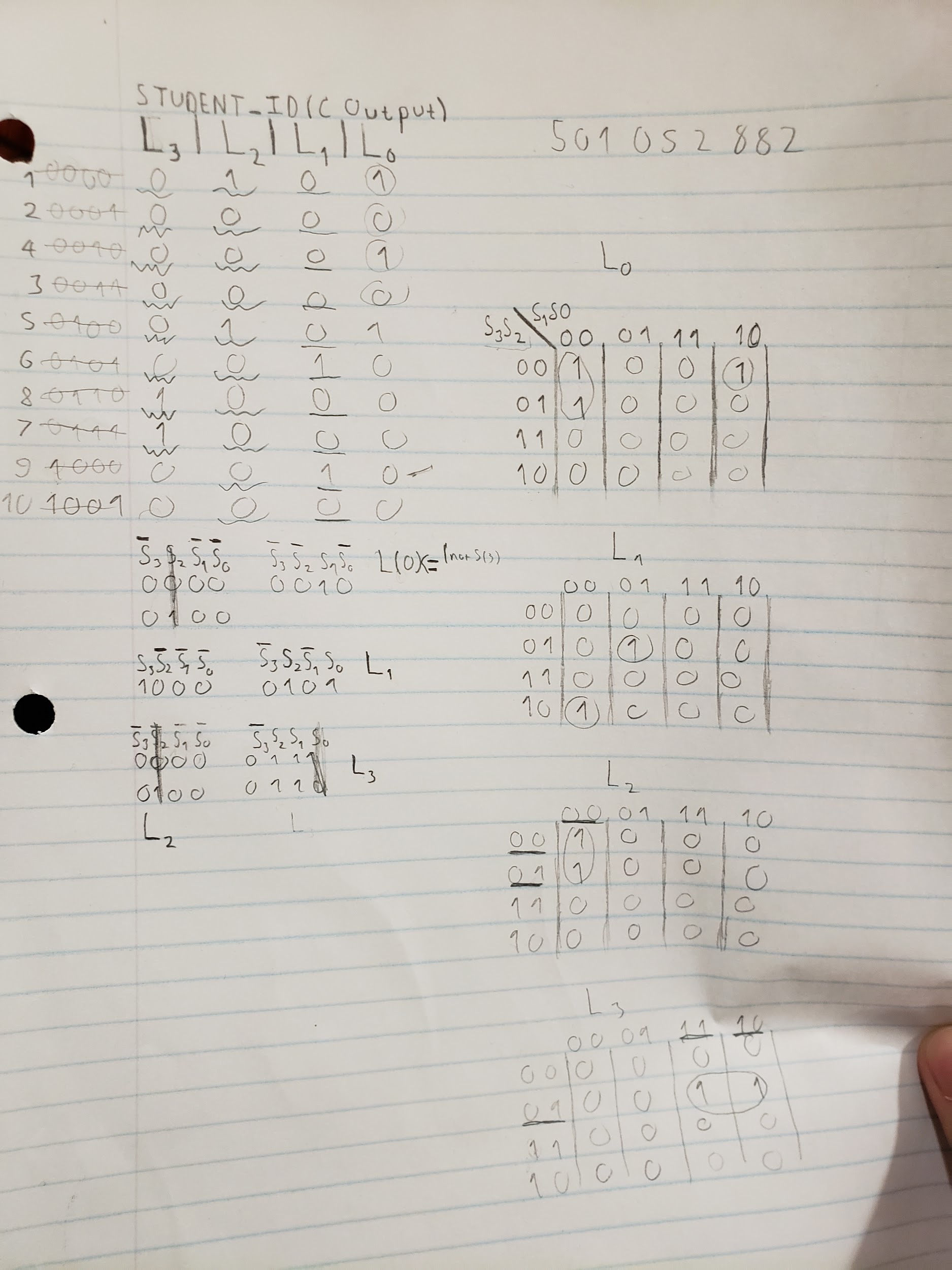


This is a picture of our block diagram schematics for part 1 of lab 3 with the symbols of the VHD code

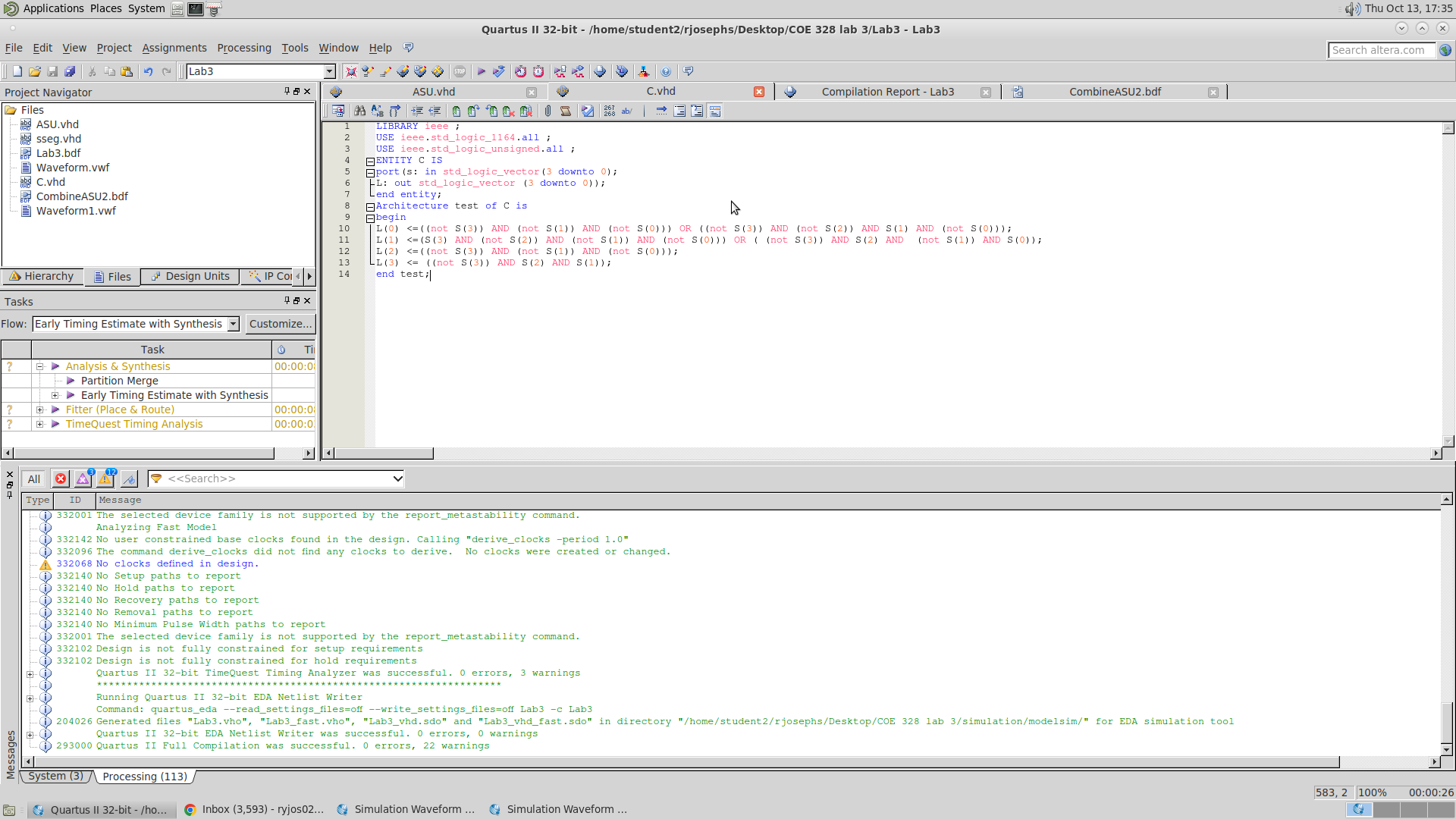


This is our Waveform outputs for part 1 of lab 3 with computer software Quartus II 13.0 

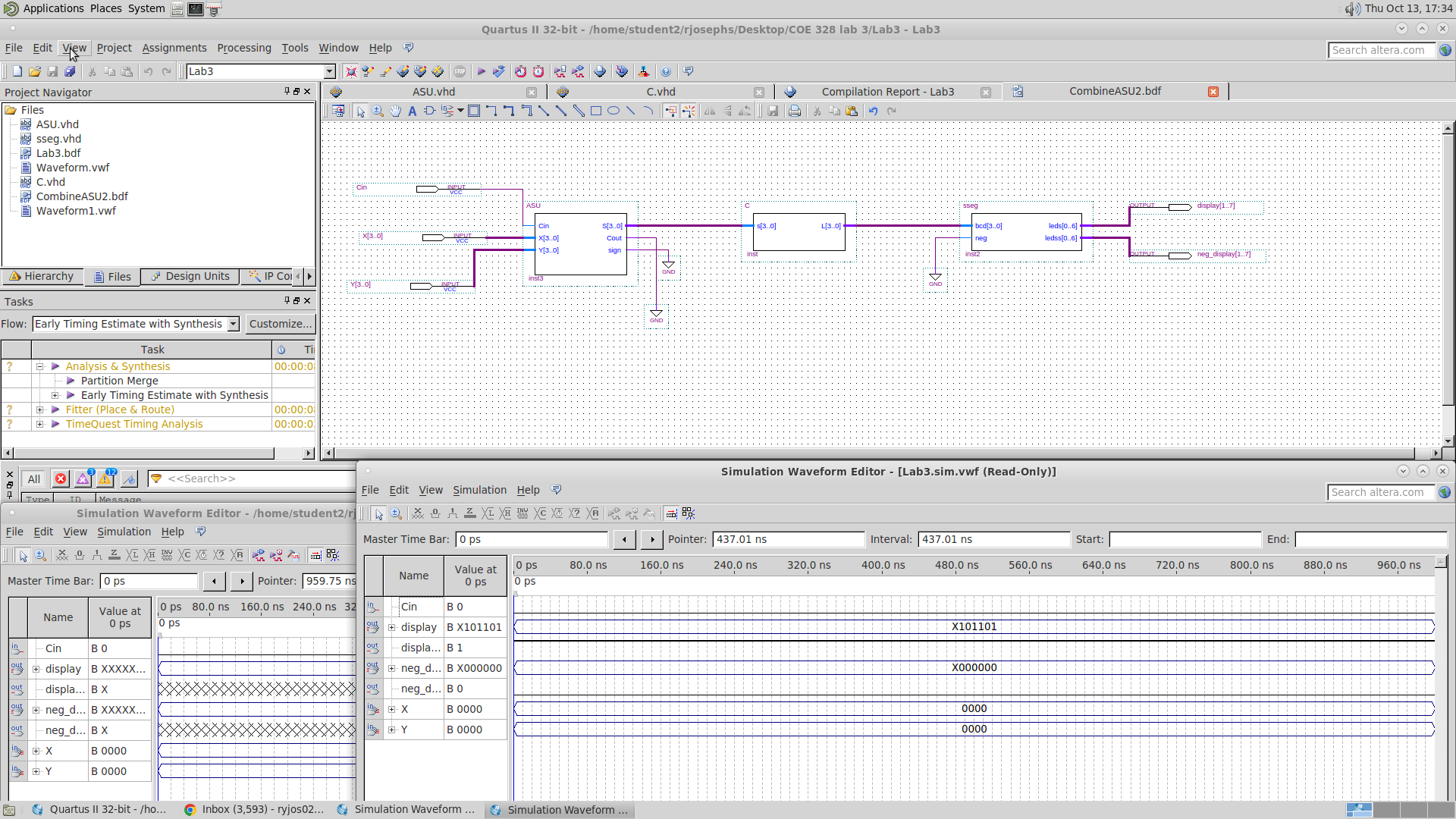
These are our 4 kmaps for part 2 of lab 3 using the student #501052882



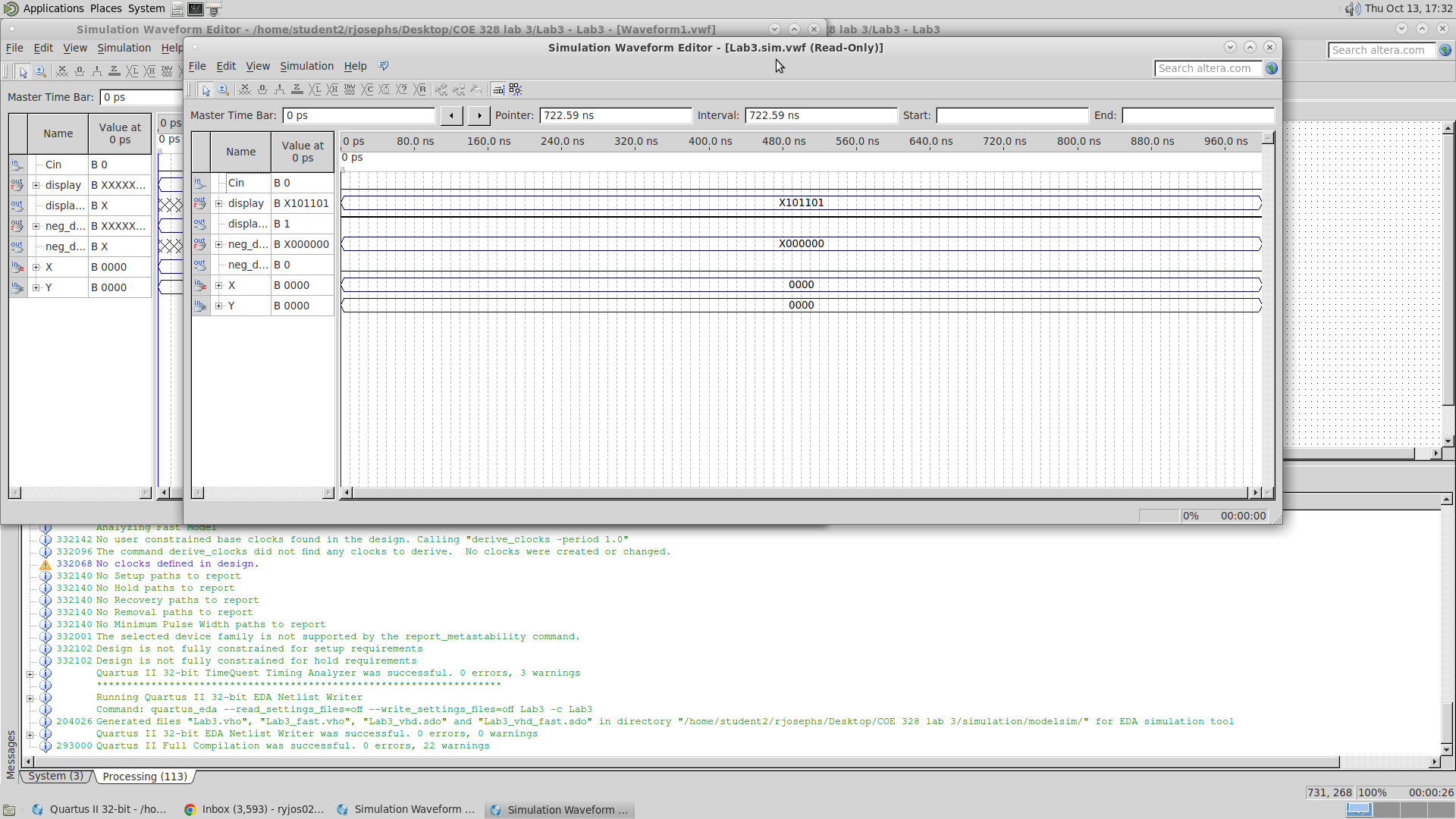
This is our vhd Skeleton code for our kmap created in part 2 of lab 3



This is a picture of our block diagram schematics for part 2 of lab 3 with the symbols of the VHD code



This is our Waveform outputs for part 2 of lab 3 with computer software Quartus II 13.0



**Conclusion:**

To wrap up our lab 3, we designed and implemented a 4-bit Adder/Subtractor unit (ASU) and the Adder/Subtractor unit that multiplexes add and subtract operations with a standard Cin input. This was done by modifying the 4-bit Adder/Subtractor unit and seven-segment VHDL code, then creating a block diagram schematics with the symbols and then getting a waveform output of it. Then in lab 3, part 2, using combinational logic, we created our four k-maps with the nine digits of our student number; and a new VHDL file which implements the logic expressions. Another schematic with the new symbol was created, and then we got the waveform output of it.